What is claimed is:

1. An electronic apparatus having a semiconductor integrated circuit having a first circuit and a second circuit, each of the first circuit and the second circuit having a normal operation state and a standby state, the electronic apparatus comprising:

power controlling means for supplying power to the first circuit and the second circuit in the normal operation state and for supplying power to only the first circuit in the standby state;

clock controlling means for controlling generation of a first clock and a second clock so as to generate the first clock and the second clock in the normal operation state and only the first clock in the standby state;

a first register that is disposed in the first circuit and operated with the first clock;

a second register that is disposed in the first circuit and operated with the second clock; and

controlling means for copying contents that are set to the first register to the second register when the state changes from the standby state to the normal operation state.

2. The electronic apparatus as set forth in claim 1,

wherein the frequency of the first clock is lower than the frequency of the second clock.

3. The electronic apparatus as set forth in claim 1,

wherein data is set to the second register not through the first region in the normal operation state.

4. The electronic apparatus as set forth in claim 1,

wherein the contents of the second register are read by a CPU disposed in the second circuit.

5. The electronic apparatus as set forth in claim 1,

wherein information of an event is set from an input device disposed outside the semiconductor integrated circuit to the first register.

6. The electronic apparatus as set forth in claim 1,

wherein the power is supplied from a battery.

7. The electronic apparatus as set forth in claim 1,

wherein the contents that have been set to the first register are copied to the second register in parallel in one period of the first clock.

8. A method for controlling a semiconductor integrated circuit having a first circuit and a second circuit, each of the first circuit and the second circuit has a normal operation state and a standby state, the method comprising the steps of:

controlling power supplied to the first circuit and the second circuit so as to supply the power to the first circuit and the second circuit in the normal operation state and the power to only the first circuit in the standby state;

controlling generation of a first clock and a second clock so as to generate the first clock and the second clock in the normal operation state and to generate only the first clock in the standby state; and

copying contents that are set in the first register that is disposed in the first circuit and operated with the first clock to a second register that is disposed in the first circuit and operated with the second clock when the state changes from the standby state to the normal operation state.